

Viasat, Inc.	Process Area: Quality	Document Number: PR001930	Revision: 005
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1 Scope

The following provides workmanship criteria related to the application of staking epoxy, conformal coating and certain other types of workmanship criteria defined herein. This criterion shall be used by the Contract Manufacturer, in addition to Viasat personnel when performing related rework, and the on-site Viasat Source Inspectors or Viasat Receiving Inspection personnel.

This criterion is general in nature and may not be suitable for all PWAs. The use of this criterion should be reviewed and determined to be applicable for each specific PWA. This review should be done by Design and Quality Engineering. Other disciplines should also review if deemed necessary. In the event it is determined to be appropriate this document shall be called out on the PWA drawing.

2 Order of Precedence

In the event of conflict between the engineering drawing, this criterion, and IPC-A-610 the following order of precedence (for the workmanship items contained herein only) shall be followed. Any exceptions to this shall be approved by the applicable Design and Quality Engineer.

- a) Engineering Drawing
- b) This workmanship criterion
- c) IPC-A-610
- d) IPC-HDBK-830

3 References

Table 1 lists the documents applicable to this Plan. Documents are the latest revision unless otherwise noted.

Table 1 - Applicable Documents

Document Title	Document Number
Acceptability of Electronic Assemblies	IPC-A-610
Guidelines for Design, Selection and Application of Conformal Coatings	IPC-HDBK-830
Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies	IPC-CC-830

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4 Acronyms Used in this Document

Acronyms	Definition
BOM	Bill of Material
EMS	Electronic Manufacturing Service provider
LED	Light Emitting Diode
PQE	Product Quality Engineer
PWA	Printed Wiring Assembly
PWB	Printed Wiring Board
SMT	Surface Mount Technology

5 General Staking Guidelines:

- 5.1 Viasat uses an "X" to denote stake locations on engineering drawings. Every effort shall be made to apply the epoxy where these locations are shown. However, in the event placement of the epoxy at the "X" location is over a Test point, the epoxy may be re-located along the same side of the component. Every effort shall be made to keep the epoxy stake locations diametrically opposed to each other. One exception to this is for BGAs and similar component package types. Staking shall be located where indicated on the drawing with an X regardless if this will cover a Test point or not.
- 5.2 Staking for SMT components is 25% to 50% of the component height. For rectangular components, which are typically staked at the corners, the staking height shall be 25% minimum to 100% maximum of the component height. See section 8.1 of IPC-A-610 for other staking requirements.
- 5.3 At no time can the staking epoxy exceed the height of the component.
- 5.4 Epoxy volume will vary depending on component type and shape. In all instances a clear bonding area between the component and the mounting surface (typically the PWB surface) should be evident. Minimum width of epoxy bond line shall be 0.02".

6 Epoxy Staking Requirements

- 6.1 The EMS may use SMT reflow epoxy to hold specific components in place during SMT reflow. The use of this epoxy shall not be cause for rejection provided it meets the requirements listed below.
 - 6.2 For component staking epoxy the following applies:
 - a) Connectors
 - All mating areas of connectors shall be free of staking epoxy.
 - b) Epoxy on component leads, vias, pads, conductors or Test points (denoted as TP#, PP#, or) within 0.250" of a stake site is permitted except as noted below. At no time can the presence of staking material interfere with the formation of a solder joint.
 - The one exception to this permission is if the board has an exposed metal area designed for fence/shield or cover contact. These areas must always be free of all epoxy.
 - c) Staking epoxy shall not completely obscure component reference designators. If epoxy partially obstructs reference designators it is acceptable if the reference designator can still be read.
 - 6.3 See sample photos S1, S2, S2.A, S3, S4 & S5 for examples of acceptable epoxy applications.
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7 Conformal Coating Guidelines

7.1 From IPC-HDBK-830:

- a) The Design Activity is to specify the areas of 'where to' and 'where not to' coat with consideration of the end use environment. The following are some factors to be considered:
- All solder joints and exposed leads should be coated.
 - Bare board areas with no traces or joints are not necessary to coat, but may be considered optional, if for cosmetic purposes only.
 - Coating for cosmetic reasons may adversely affect assembly cycle time and usage cost.
 - Component packaging

8 Conformal Coating Requirements

- 8.1 See section 10.8 of IPC-A-610 for acceptability requirements:
- 8.2 All electrically conductive elements shall be covered with conformal coating except exposed metal area designed for fence/shield or cover contact.
- 8.3 Coating of the bodies of encased relays, insulated or encapsulated devices, or ceramic components, is optional unless otherwise specified on the drawing.
- 8.4 Coating tolerance of +/- 0.020" is allowed between boundary areas of keep-out zones unless otherwise specified on the drawing or unless electrically conductive elements would be left uncoated (see section 8.2).
- 8.5 Coating edges where the masking material has been removed shall be free from roughness, tears, or breaks having a linear dimension greater than 0.05 inch in height, length, or width from any edge.
- 8.6 Rough edges which appear along previously masked areas shall not be cause for rejections unless adjacent circuit traces, pads or component leads are exposed.
- 8.7 Webbing is a membrane of coating suspended between component bodies, component leads, component bodies to the PWB laminate surface, and/or component leads to the PWB laminate surface, and is generally concave in appearance. Webbing shall not be cause for rejection.
- 8.8 Connectors
- a) All accessible soldered leads of connectors shall be conformal coated (for example connectors with thru-hole leads underneath the connector body cannot be coated as the leads are not accessible).
- b) All mating areas of connectors shall be free of conformal coat.
- c) All non-conductive areas of connectors do not require conformal coating, but may be coated.
- 8.9 Standoffs
- a) Coating of standoffs is optional; however, the mating surface of standoffs shall NOT be coated.
- b) Coating of threads in a threaded standoff is prohibited.
- 8.10 LEDs
- a) The solder leads of LEDs shall be covered with conformal coat if accessible.
- 8.11 Test Points (Reference Designators TP#, PP#, or)
- a) Test points shall be covered with conformal coat.
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9 Conformal Coat Rework

- 9.1 If a gel stripper is used to remove conformal coat extreme care must be exercised to prevent tarnishing of gold plated areas on PWAs. Tarnishing of gold plated areas is not acceptable. Tarnish is an oxide layer on a metal surface that causes it to dull, often discoloring it.

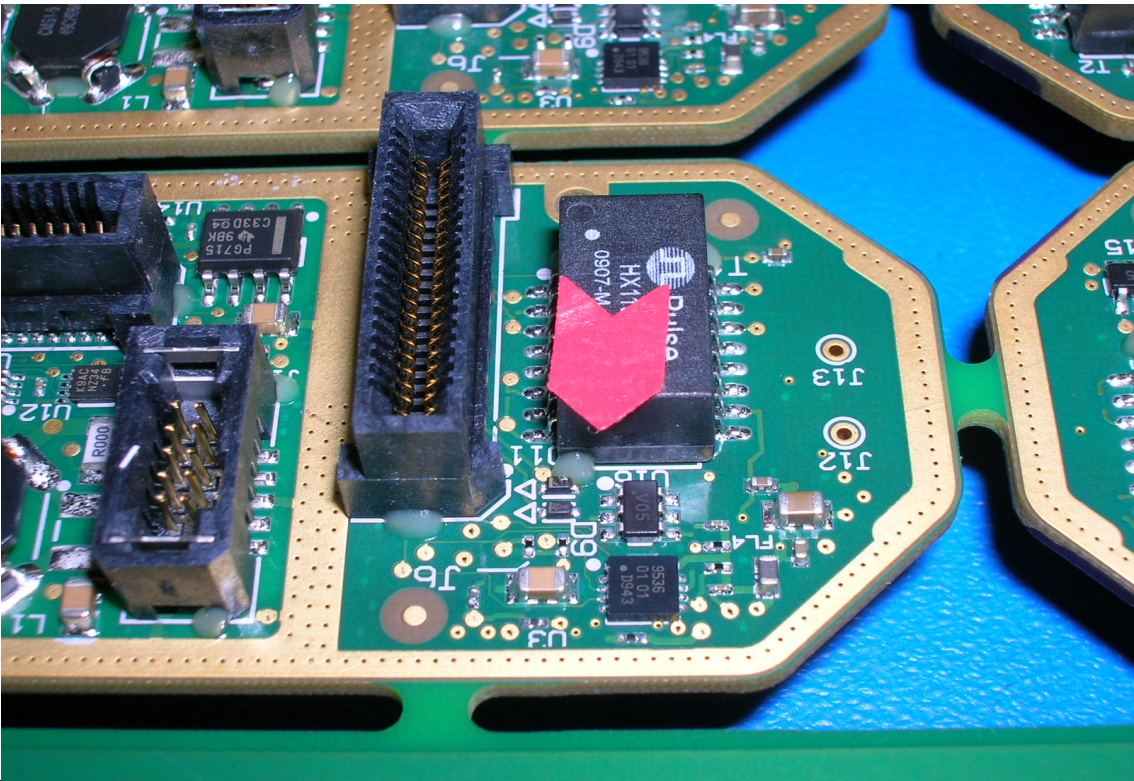
10 Solder on exposed metal fence area


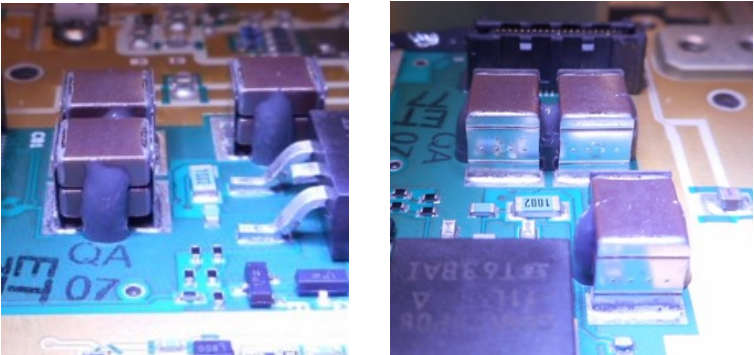
- 10.1 Every effort shall be made to prevent solder from coming into contact with an exposed metal fence area. These areas are typically critical seating areas for EMI gaskets.
- 10.2 In the event solder does come in contact with this area the following guidelines shall be followed.
- a) Solder splash shall not exceed 0.5" in its longest dimension.
 - b) The solder splash area must be "flat" to the touch. "Flat" in this context means the solder splash area should be undiscernible by touch when you run the end of an orangewood stick at a 45 degree angle over the solder splash area.
 1. The following is a requirement
 - a. The EMS shall contact the Viasat quality engineer for disposition.
 2. See sample photo #F1.

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11 Appendix A

The table below provides several examples of items that have been evaluated and may or may not be cause for rejection. See the Technical Findings column. The Contract Manufacturer should contact the assigned PQE if there are any questions.

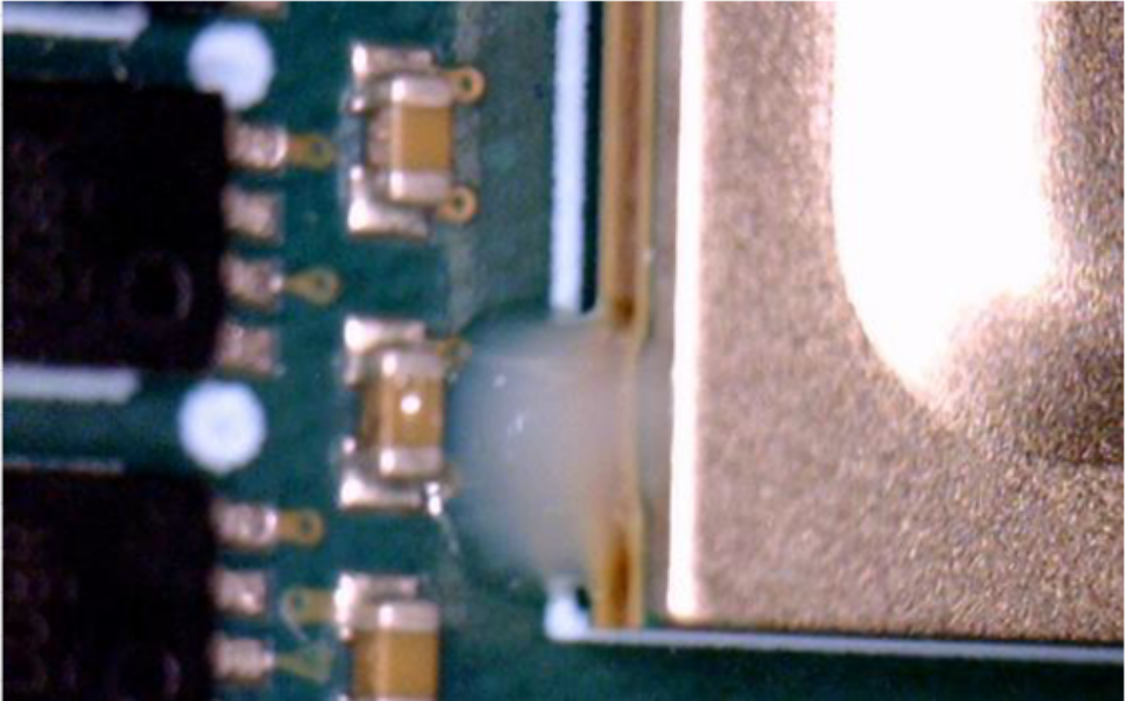
P/N and Description	Issue Description	Technical Findings	Sample photos
All PWAs	Epoxy migration	Acceptable for Class 2 & 3 provided epoxy migration is within 0.250" of epoxy stake site.	<p>SAMPLE PHOTO #S1</p> 

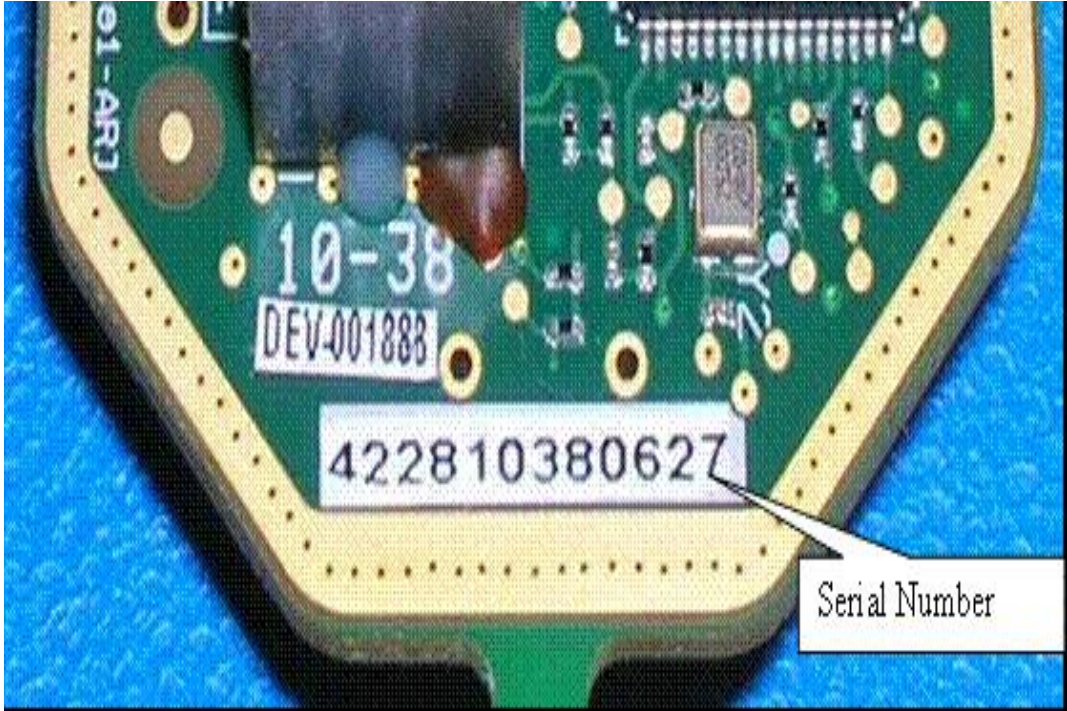
P/N and Description	Issue Description	Technical Findings	Sample photos
All PWAs	Epoxy migration	Acceptable for Class 2 & 3 provided epoxy migration is within 0.250" of epoxy stake site.	<p>SAMPLE PHOTO #S2</p> 
All PWAs	Stacked Capacitors	Acceptable for Class 2 & 3 provided that epoxy is a minimum of 50% the height of the top capacitor	<p>SAMPLE PHOTO #S2.A</p> 

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P/N and Description	Issue Description	Technical Findings	Sample photos
All PWAs	Epoxy Migration	Acceptable for Class 2 & 3 provided epoxy migration is within 0.250" of epoxy stake site.	<p>SAMPLE PHOTO #S3</p> 

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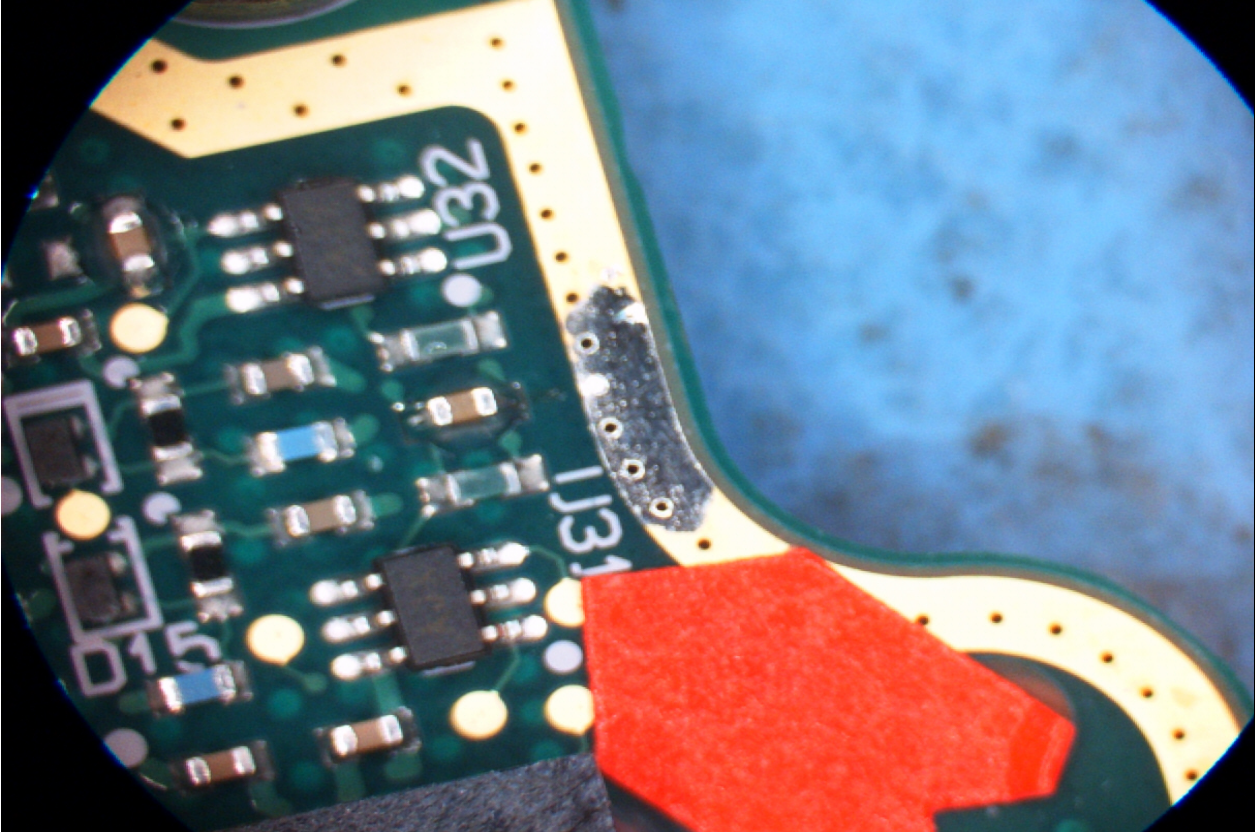
P/N and Description	Issue Description	Technical Findings	Sample photos
All PWAs	Epoxy Migration	Acceptable for Class 2 & 3 provided epoxy migration is within 0.250" of epoxy stake site.	SAMPLE PHOTO #S4 

P/N and Description	Issue Description	Technical Findings	Sample photos
All PWAs	Presence of SMT Epoxy	Acceptable for Class 2 & 3	<p>SAMPLE PHOTO #S5</p> 

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P/N and Description	Issue Description	Technical Findings	Sample photos
All PWAs	Staking Adhesive residue	Acceptable provided none is seen using naked eye inspection. Inspect at approx. 18" using ambient lighting. Rejectable if adhesive residue is seen with the naked eye.	None
All PWAs	Misplaced epoxy (not staked per this spec)	Reject	None

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P/N and Description	Issue Description	Technical Findings	Sample photos
PWAs with exposed metal fence	Solder on exposed metal fence area	Reject if surface is not flat. Acceptable for Class 2 & 3 if surface is flat <u>and</u> approved by Viasat Quality Engineer.	<p>SAMPLE PHOTO #F1</p>  <p>A microscopic photograph of a green printed circuit board (PCB) showing various electronic components. A red arrow points to a specific area where solder is applied to a metal fence. The solder appears to be on a raised surface, which is the issue being documented. The background is a blurred blue color.</p>